



2184 #4  
ATTORNEY DOCKET NO. 010541  
12-47

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of )

- Butler et al. )

For: ERASURE-AND-SINGLE-ERROR  
CORRECTION DECODER FOR  
LINEAR BLOCK CODES

Serial No. 10/010,199 )

) Examiner: Tonya Lee

Filed: December 4, 2001 )

) Group No. 2184

INFORMATION DISCLOSURE STATEMENT

RECEIVED

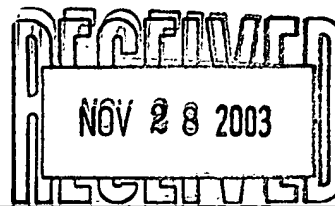
NOV 26 2003

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Technology Center 2100

Dear Sir:

Applicants submit herewith, in accordance with 37 CFR § 1.98, the patents, publications and other information listed on the enclosed Form PTO-1449.



CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

MAILING

- ☒ deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

FACSIMILE

- ☐ transmitted by facsimile to the Patent and Trademark Office.

Depositor's Name: Keely Culver

Signature: Keely Culver

Date: November 19, 2003

The references submitted herewith are those of which Applicants are aware, which they believe may be material to the examination of this application and, with respect to which there may be a duty to disclose in accordance with 37 CFR § 1.56. While the references identified may be material to the examination of this application pursuant to 37 CFR § 1.56, the citation of these references is not intended to constitute an admission that any reference referred to herein is prior art to the invention of this application, unless specifically designated as such. Additionally, the filing of this Information Disclosure Statement shall not be construed to mean that any search has been made or, that if made, such search was complete or exhaustive, or that no other material information as defined in 37 CFR § 1.56 exists.

- ☒ The undersigned hereby certifies that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three month prior to the filing of this Information Disclosure Statement, therefore, no fees are believed to be due.

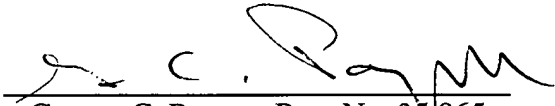
Also enclosed for your convenience is a copy of the International Search Report.

A list of the references is set forth on Form PTO-1449, which is enclosed herewith, along with a copy of each cited reference. Applicants respectfully request that the Examiner return to Applicants a copy of the Form PTO-1449 indicating consideration of the references cited thereon.

Applicants do not believe that any fees are due. If, however, it is determined that fees are owed, Applicants hereby authorize that such fees be charged to Deposit Account No. 17-0026.

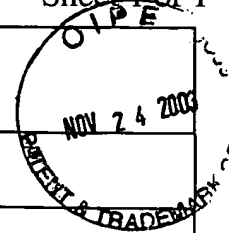
Respectfully submitted,

Dated: November 19, 2003

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE (REV. 7-80) PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 010544	SERIAL NO. 10/010,199
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT Butler et al.	
		FILING DATE December 4, 2001	GROUP 2184
DATE MAILED: November 19, 2003			



## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPRO- PRIATE
	A1						
	A2						
	A3						
	A4						
	A5						

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS
	B1	0 4 0 7 1 0 1 A2	01/09/91	EP	Digital Equipment Corp.	G11B	20/18
	B2						
	B3						

## OTHER PRIOR ART (Including Author, Title, Date, Pertinent Page, Etc.)

	C1	Katayama, Y et al: "One-Shot Reed-Solomon Decoding For High-Performance Dependable Systems", 2000 IEEE International Networks, NY, USA, June 25, 2000, pages 390-399.
	C2	Alzahrani, F et al: "On-Chip TEC-QED ECC For Ultra-Large, Single-Chip Memory Systems", Proceedings IEEE International Conference On Computer Design, October 10, 1994, pages 132-137.
	C3	Franklin, M et al: "Theory and Techniques For Testing Check Bits Of Rams With On-Chip ECC", IEICE Transactions On Information and Systems, Tokyo, Japan, Volume E76-D, No. 10, October 1, 1993, pages 1243-1252.
	C4	Nagvajara, P : "Multichip Module Diagnosis, Electro/94 International Conference Proceedings, Boston, MA, IEEE, USA. Combined Volumes, May 10, 1994, pages 793-802.
EXAMINER		DATE CONSIDERED
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		